

#### Features

- 10.2 Gb/s HDMI 1.3 compatible
- 10.8 Gb/s DisplayPort V1.0 compatible
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

#### Applications

- Multi-rate HDMI interfaces
- Multi-rate DisplayPort interfaces

#### Description

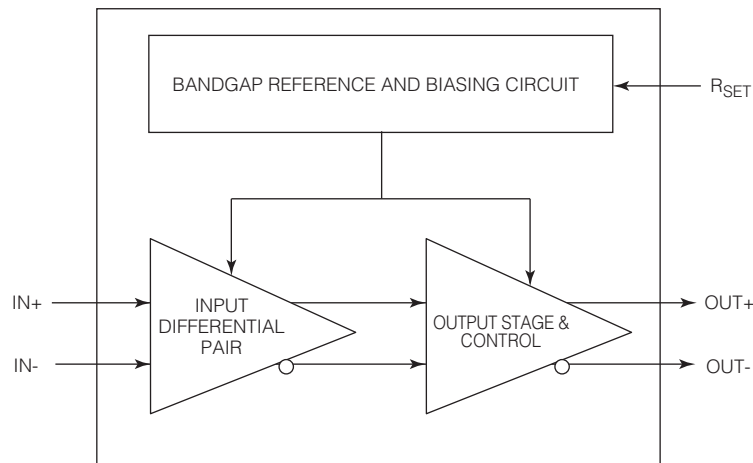
The GV8500 is a high-speed BiCMOS integrated circuit designed to drive 75Ω co-axial cables.

The GV8500 may drive data rates up to 3.4Gb/s for HDMI and DisplayPort applications.

The GV8500 accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 168mW using a 3.3V power supply. The GV8500 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



**GV8500 Functional Block Diagram**

# Contents

Features .....	1
Applications .....	1
Description .....	1
1. Pin Out .....	3
1.1 Pin Assignment .....	3
1.2 Pin Descriptions .....	3
2. Electrical Characteristics .....	4
2.1 Absolute Maximum Ratings .....	4
2.2 DC Electrical Characteristics .....	4
2.3 AC Electrical Characteristics .....	5
2.4 Solder Reflow Profiles .....	6
3. Input / Output Circuits .....	7
4. Detailed Description .....	8
4.1 Input Interfacing .....	8
4.2 Output Interfacing .....	8
4.2.1 Output Amplitude (RSET) .....	8
5. Application Information .....	8
6. Package & Ordering Information .....	9
6.1 Package Dimensions .....	9
6.2 Recommended PCB Footprint .....	10
6.3 Packaging Data .....	10
6.4 Marking Diagram .....	11
6.5 Ordering Information .....	11
7. Revision History .....	12

# 1. Pin Out

## 1.1 Pin Assignment

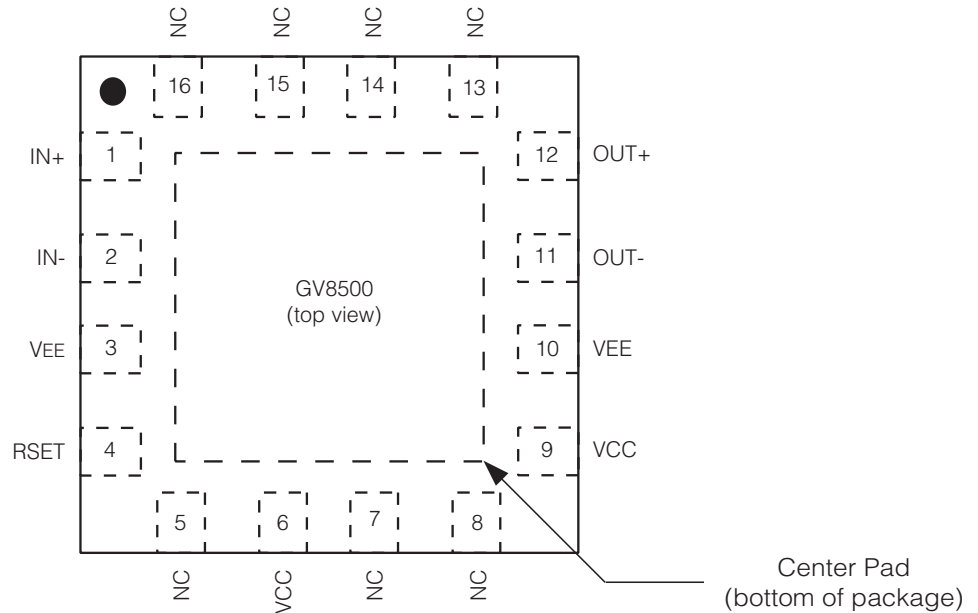


Figure 1-1: 16-Pin QFN

## 1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	IN+, IN-	Analog	Input	Differential inputs.
3,10	V <sub>EE</sub>	–	Power	Most negative power supply connection. Connect to GND.
4	R <sub>SET</sub>	Analog	Input	External output amplitude control resistor.
5,7,8,13 14,15,16	NC	–	–	No Connect.
6,9	V <sub>CC</sub>	–	Power	Most positive power supply connection. Connect to +3.3V.
11,12	OUT-, OUT+	Analog	Output	Differential outputs.
–	Center Pad	–	Power	Connect to most negative power supply plane following the recommendations in <a href="#">Recommended PCB Footprint on page 10</a> .

## 2. Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V <sub>DC</sub>
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T <sub>s</sub> < 125°C
Input Voltage Range (any input)	-0.3 to (V <sub>CC</sub> +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

### 2.2 DC Electrical Characteristics

**Table 2-1: DC Electrical Characteristics**

V<sub>CC</sub> = 3.3V ±5%; T<sub>A</sub> = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	–	3.135	3.3	3.465	V
Power Consumption	P <sub>D</sub>	T <sub>A</sub> = 25°C	–	168	–	mW
Supply Current	I <sub>s</sub>	T <sub>A</sub> = 25°C	–	51	–	mA
Output Voltage	V <sub>CMOUT</sub>	Common mode	–	V <sub>CC</sub> - V <sub>OUT</sub>	–	V
Input Voltage	V <sub>CMIN</sub>	Common mode	1.4 + ΔV <sub>DDI</sub> /2	–	V <sub>CC</sub> - ΔV <sub>DDI</sub> /2	V

## 2.3 AC Electrical Characteristics

**Table 2-2: AC Electrical Characteristics**

$V_{CC} = 3.3V \pm 5\%$ ;  $T_A = 0^\circ C$  to  $70^\circ C$ , unless otherwise shown

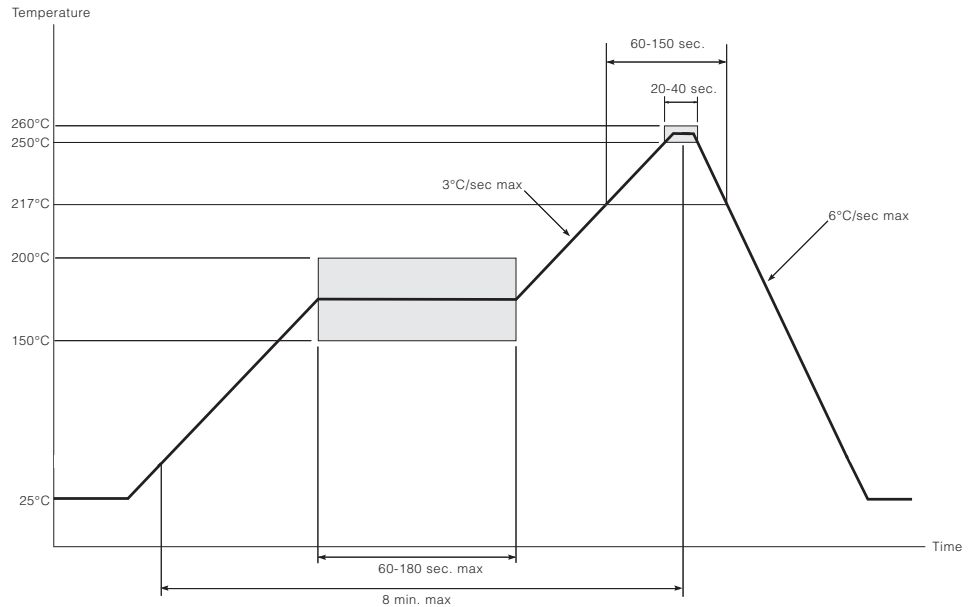
Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR	–	0.25	–	3.4	Gb/s	1
Serial Input Clock Rate	–	HDMI Clock, 1/10th Data Rate	25	–	340	MHz	–
Additive Jitter	–	3.4Gb/s	–	22	–	ps <sub>p-p</sub>	–
	–	1.5Gb/s	–	20	–	ps <sub>p-p</sub>	–
Rise/Fall Time	$t_r, t_f$	–	–	–	135	ps	2
Mismatch in Rise/Fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	30	ps	3
Overshoot	–	–	–	–	10	%	3
Output Voltage Swing	$V_{OUT}$	$R_{SET} = 750\Omega$	750	800	850	mV <sub>p-p</sub>	3
Input Voltage Swing	$\Delta V_{DDI}$	Differential	400	–	1560	mV <sub>p-p</sub>	–

NOTES:

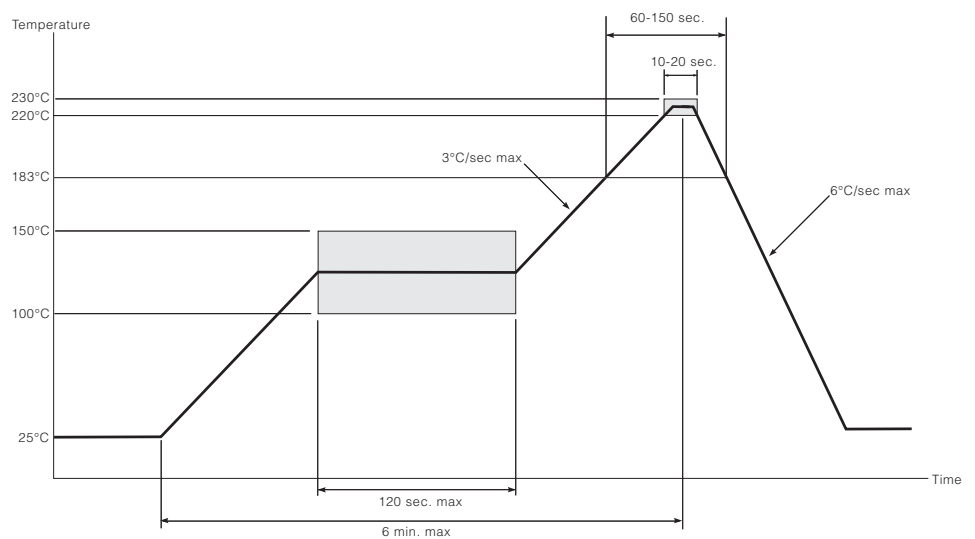
1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.
3. Single Ended into  $75\Omega$  external load.

## 2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in [Figure 2-1](#). The recommended standard Pb reflow profile is shown in [Figure 2-2](#).



**Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)**



**Figure 2-2: Standard Pb Reflow Profile**

### 3. Input / Output Circuits

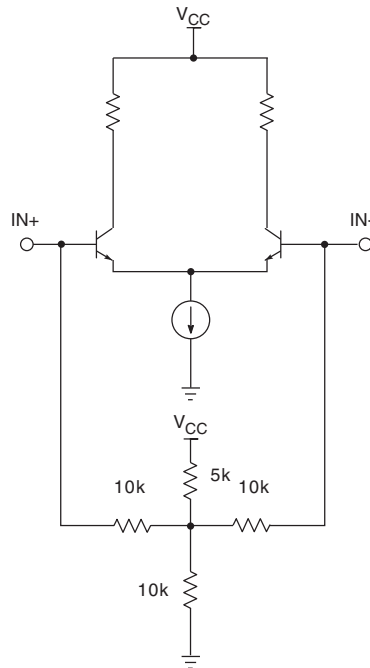


Figure 3-1: Differential Input Stage (IN+/IN-)

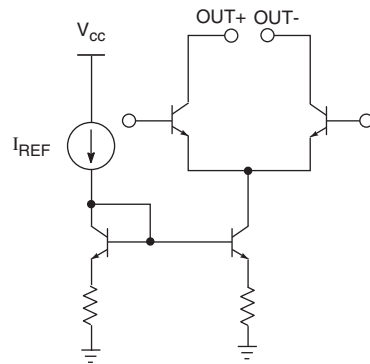


Figure 3-2: Differential Output Stage (OUT+/OUT-)

## 4. Detailed Description

### 4.1 Input Interfacing

IN+/IN- are high impedance differential inputs. The equivalent input circuit is shown in [Figure 3-1](#).

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 400 and 1560mVpp.
- The common mode voltage range must be as specified in the [DC Electrical Characteristics on page 4](#).
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GV8500 inputs are self-biased, allowing for simple AC coupling to the device.

### 4.2 Output Interfacing

The GV8500 outputs are current mode, and will drive typically 800mV into a 75 $\Omega$  load. These outputs are protected from accidental static damage with internal ESD protection diodes.

#### 4.2.1 Output Amplitude (RSET)

The output amplitude of the GV8500 is set by the value of the R<sub>SET</sub> resistor. In order to produce an 800mV<sub>p-p</sub> output with a nominal  $\pm 7\%$  tolerance, a value of 750 $\Omega$  is required. A  $\pm 1\%$  SMT resistor should be used.

The R<sub>SET</sub> resistor is part of the high speed output circuit of the GV8500. The resistor should be placed as close as possible to the R<sub>SET</sub> pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R<sub>SET</sub> resistor and the R<sub>SET</sub> pin.

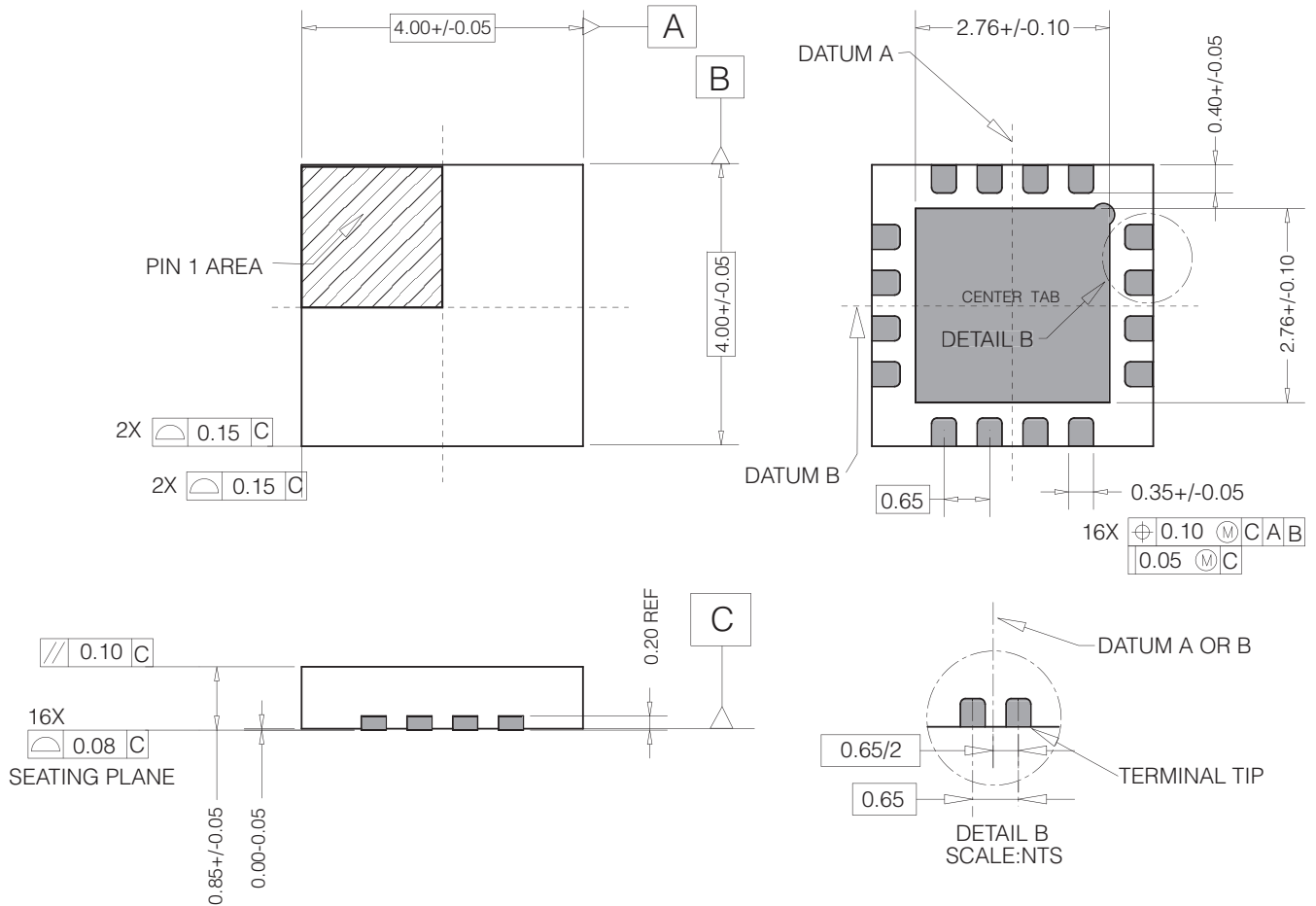
## 5. Application Information

Contact [vbapps@gennum.com](mailto:vbapps@gennum.com) for information

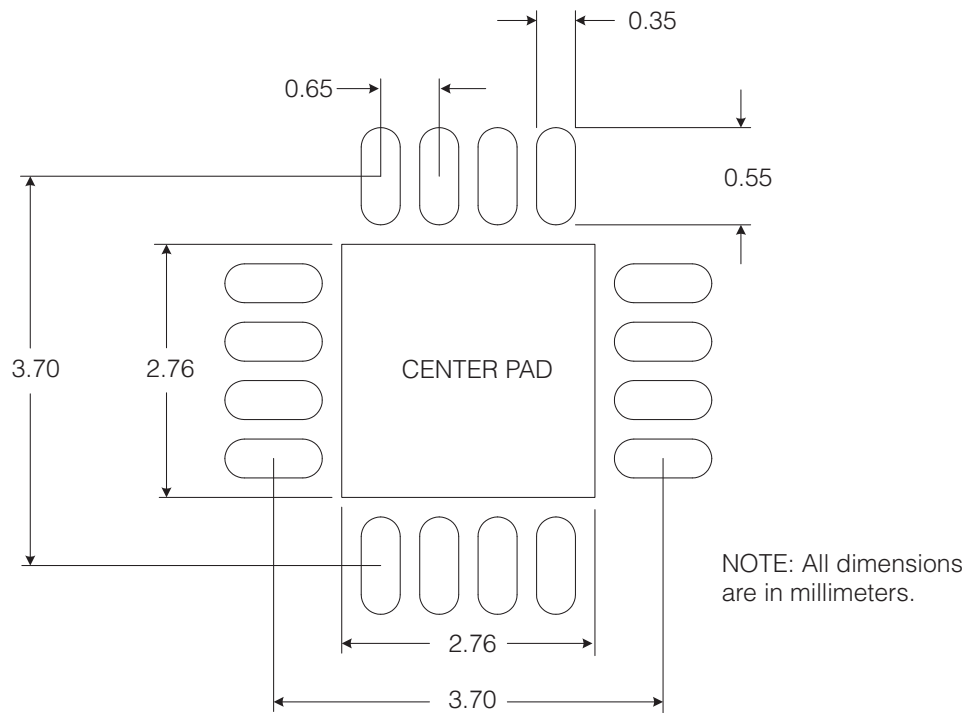


# 6. Package & Ordering Information

## 6.1 Package Dimensions



## 6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

## 6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, $\theta_{j-c}$	31.0°C/W
Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow)	43.8°C/W
Psi, $\Psi$	11.0°C/W
Pb-free and RoHS compliant	Yes

### 6.4 Marking Diagram

Pin 1 Indicator



XXXX - Lot/Work Order ID  
 YYWW - Date Code  
 YY - 2-digit year  
 WW - 2-digit week number

### 6.5 Ordering Information

	Part Number	Package	Temperature Range
GV8500	GV8500-CNE3	16-pin QFN	0°C to 70°C

## 7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
A	148086	–	October 2007	New document.

### CAUTION

ELECTROSTATIC SENSITIVE DEVICES  
DO NOT OPEN PACKAGES OR HANDLE  
EXCEPT AT A STATIC-FREE WORKSTATION



### DOCUMENT IDENTIFICATION ADVANCE INFORMATION NOTE

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### GENNUM CORPORATION

Mailing Address: P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3  
Shipping Address: 970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5  
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

### GENNUM JAPAN CORPORATION

Shinjuku Green Tower Building 27F, 6-14-1, Nishi Shinjuku, Shinjuku-ku, Tokyo, 160-0023 Japan  
Tel. +81 (03) 3349-5501, Fax. +81 (03) 3349-5505

### GENNUM UK LIMITED

25 Long Garden Walk, Farnham, Surrey, England GU9 7HX  
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523

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